ABSTRACT OF DISCLOSURE

A fractional-N synthesizer with programmable output phase including a phase locked loop having an output signal whose frequency is a fractional multiple of an input reference signal, the phase locked loop including a frequency divider. A synchronization circuit responsive to the input reference signal for generating synchronization pulses at integer multiples of M periods of the input reference signal. An interpolator is responsive to an input fraction F/M, where F is the fractional value, to provide to the frequency divider an output which is a fractional value equal to, on average, the input fraction. A phase adjustment circuit is responsive to the synchronization circuit for varying the phase of the output signal with respect to the input reference signal.